Design of Piezoelectric Transformers for Power Converters by Means of Analytical and Numerical Methods

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***Abstract*—Piezoelectric transformers (PTs) provide several advantages compared to magnetic components, which are higher power density, lower radiated noise, and higher voltage isolation capability. PT must be properly designed to benefit the power converter with the aforementioned advantages. Analytical models are widely used for PT design in order to validate it before constructing the prototype. In this paper, the additional usefulness of finite element analysis (FEA) for PT design is shown. With FEA, it is possible to optimize the PT design not only by maximizing the energy transference but also by cleaning the working frequency range of spurious modes (geometrical 2-D/3-D effects). Moreover, FEA tools allow the study of other main aspects of the PT design such as manufacturing tolerances or the influence of the fixing layer on PT performance (which is a critical design point). A method for modeling and designing PTs is proposed, combining analytical 1-D models and FEA results. The proposed method is validated with measurements of a PT design for a 10-W ac/dc converter prototype for mobile phone battery charger.**

***Index Terms*—Design methodology, finite element methods, piezoelectric transformer (PT), power conversion.**

I. Introduction

NOWADAYS, piezoelectric transformers (PTs) become, in some applications, an alternative to the magnetic transformers for power supplies, when system miniaturization, high voltage conversion ratio, high isolation voltages, and low EMI content are critical design points [1]–[3]. In order to benefit the application with the PT advantages, PT design should be realized by taking into account power converter topology restrictions. Although PT is penalized in terms of efficiency and size, it is possible to eliminate the additional magnetic elements (impedance matching) [4].

The analytical equations which describe the PT behavior are difficult to be solved as a 3-D system [5]. Most designers do a simplification by considering the vibration of the PT in only one direction (1-D models), but displacements in different and nondesired directions (2-D/3-D effects) may exist. These spurious modes imply a reduction in PT efficiency. With analytical 1-D models, it is possible to select the type of material, number of layers, thickness of each layer, area, and electrode distribution, but not the 2-D/3-D geometry. Therefore, it is necessary to use finite element analysis (FEA) tools in order to take into account 2-D/3-D effects to select the geometry for an optimum design.

The main goal in PT geometrical design is that the working frequency range (between resonance and antiresonance) must be free of spurious modes. Apart from avoiding spurious modes, another design goal is to obtain a high electromechanical coupling coefficient (k_{eff}) in order to maximize the efficiency of conversion and power transference, as can be deduced from the following equation:

$$\frac{\text{Power}}{\text{Volume}} \propto k_{\text{eff}}^2 \cdot \varepsilon \cdot f \tag{1}$$

where ε is the material permittivity, and f is the vibration frequency.

In this paper, a design method for PTs is presented as a combination between analytical (1-D models) and numerical results (FEA tools). A detailed description of the design stages of a PT will be shown using a specific example: a PT for an ac/dc converter of a mobile phone battery charger (universal input voltage, output voltage is 12 V, and output power is 10 W). Since the ac adapters for mobile phones should be as small as possible, PTs are a good candidate to achieve this goal.

II. Design Stages

The power that a PT can transfer depends on the material type and area. Total length, thickness, or diameter of the transformer is selected according to the specified working frequency. By selecting the number and thickness of the layers of the primary and the secondary side of the PT, the voltage ratio is fixed. All of these constructive parameters can be selected with an analytical 1-D model, and most of the designers stop at this stage. However, it is possible to go further with FEA. Using this way, geometry or shape is selected in order to reduce the spurious modes at the working frequency range. A critical design point is the fixing and the mounting of the PT because the performance of PT changes if its vibration is perturbed, since it is an electromechanical device. In addition, manufacturing tolerances must be taken into account because they may induce new spurious modes.

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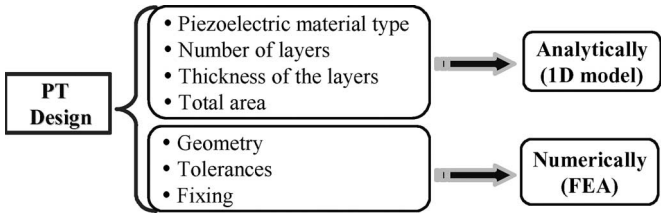

Fig. 1. Design parameters of a PT.

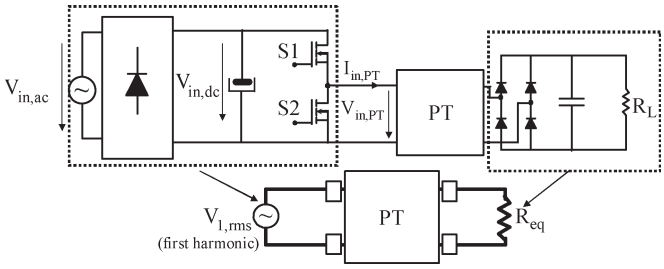

Fig. 2. Considered power converter topology (magnetic-less) and its equivalent system.

In this section, a method for PT design by combining analytical and numerical results is described by using a particular application. The different parameters required for PT design are summarized in Fig. 1.

The proposed design method has been divided into five stages: topology selection, analytical modeling and design, 2-D/3-D design and geometry selection, manufacturing tolerances influence on the PT performance, and fixing influence on the PT performance.

A. Stage A. Topology Selection

Topology must be selected by considering several aspects such as size, efficiency, EMI content, total number of components, whether magnetic components must be avoided or not, complexity of the PT driving way, etc. If the PT is sinusoidally driven, its efficiency is maximized, but the converter is penalized in terms of size because magnetic components are needed to generate this waveform. When the PT is driven with a square voltage, its efficiency is reduced, and its design is more complex; however, it is possible to obtain a magnetic-less converter. Therefore, it will also be necessary to avoid the magnetic components in the rectifier stage.

For this particular example, a half-bridge inverter (Fig. 2) is selected in terms of the required input voltage range and power level. The input ac voltage is rectified, and then, the dc voltage is transformed to a proper ac voltage to drive the PT (inverter stage). Another rectification is needed to adapt the PT output voltage (ac) to the dc voltage that must be applied to the load (R_{L}). A full-bridge rectifier has been selected since magnetic components must be avoided in this solution. As described in [6], the equivalent system of the power converter topology substitutes the inverter stage of the topology with a sinusoidal voltage corresponding to the first harmonic of the square voltage at the output of the half-bridge inverter $(V_{1,\mathrm{rms}})$. In addition, the output stage of the converter (rectifier and load) can be substituted with an equivalent resistive load (R_{eq}). The value of R_{eq} depends on the type of rectifier stage.

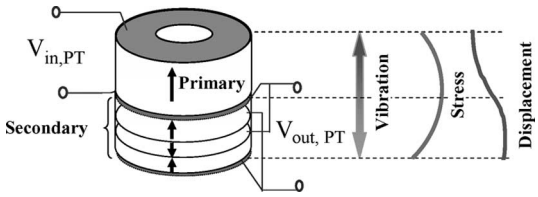

Fig. 3. Multilayer PT working in thickness mode.

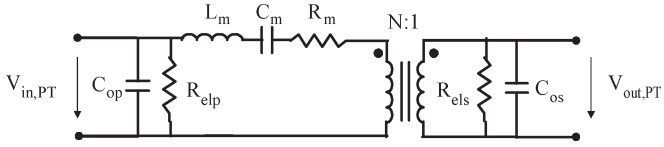

Fig. 4. Mason model.

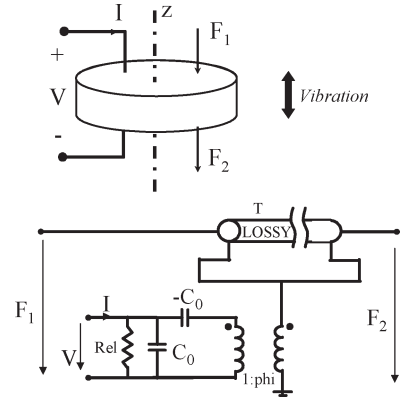

Fig. 5. Transmission line model of a piezoelectric material layer working in thickness mode.

B. Stage B. Analytical Modeling and Design

PT must also comply with the requirements at the component and converter levels. For this stage, an analytical model is very useful, which can be easily implemented in an electrical simulator like PSpice. In this particular case, PT vibration along its thickness (Fig. 3) has been selected to obtain a low-profile converter (since the operating frequency of the power converter is inversely proportional to PT thickness).

Usually, PT designers use Mason model (Fig. 4) due to its simplicity [7]. Nevertheless, the Mason model is only valid when PT is sinusoidally driven because it only takes into account the PT resonance frequency.

However, if the PT is driven with a square voltage, higher vibration orders must be taken into account. This can be achieved using the transmission-line-based model [8]. Each layer of piezoelectric material is modeled in an independent way by one circuit like the one shown in Fig. 5. With this model, different fixing conditions, poling, and position of the layers can be considered.

At the component level, the design outputs of this design step are constructive parameters such as the PT type of material, area, and lateral structure of the PT (number of layers, thickness of each layer, and electrode distribution). At the

TABLE I
INFLUENCE OF THE PT CONSTRUCTIVE PARAMETERS IN THE PT ELECTRICAL PROPERTIES

Constructive parameter	R_{opt}	Maximum G_{PT}	η_{PT}	k_{eff}	ZVS
↑ Area	Decrease	Increase	Constant	Constant	Improve
↑ Number of secondary layers	Decrease	Constant	Constant	Constant	Worsen
↑ Thickness of secondary layers	Increase	Decrease	Constant	Constant	Constant
↑ Thickness of primary layers	Constant	Decrease	Constant	Has an optimum value	Improve
↑ Number of primary layers	Constant	Increase	Constant	Constant	Improve
↑ Thickness of isolation layer	Decrease	Constant	Decrease	Decrease	--

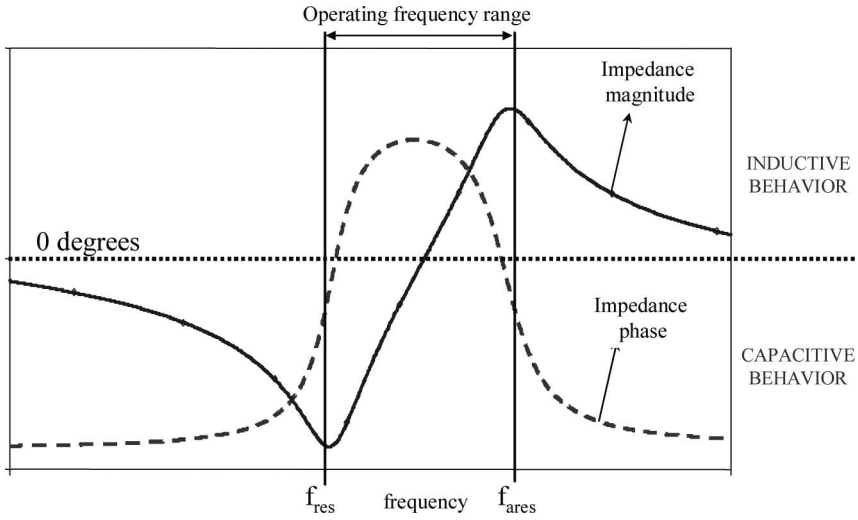

Fig. 6. Input impedance magnitude and phase versus frequency.

converter level, the design outputs are electrical parameters such as efficiency, soft switching transitions (ZVS) capability [4], transferred power, electromechanical coupling coefficient (k_{eff}), etc. Since there is no analytical relation between electrical and constructive parameters, sensitivity analysis is required in order to obtain design rules of the PT. Using these design rules, it is easy to change the physical PT structure to meet the electrical specifications of the PT. Table I summarizes the results from the sensitivity analysis that have been performed in [9]. These results show that each constructive parameter has influence in several electrical properties. Therefore, several iterations in the design process may be needed to optimize the PT in order to fulfil all the specifications. This is not a test-and-try design process, but an iterative process. There are several analytical equations that are used to define the design, but these expressions become very complex for multilayer structures and do not allow the optimization of all the parameters, especially the electrode distribution. Therefore, sensitivity analysis has been selected as a useful method in obtaining this relation.

This stage has been divided into six steps: selection of the material, selection of the PT thickness, selection of the electrode area, selection of the electrode distribution, selection of the thickness and number of secondary layers, and selection of the thickness and number of primary layers.

Step 1) Selection of the material

A lead zirconate titanate (PZT) material type has been selected due to the high value of permittivity (ε), since a higher power density can be achieved (1). In this particular example, the high input voltage value requires a material with low dielectric losses. Therefore, PZ26 of Noliac [10] has been selected.

TABLE II
PT FEATURES

Area	200 mm^2
Height	4.1 mm
Primary	2 layers x 1mm
Secondary	2 layers x 0.1mm
Bulk	2 layers x 0.95mm

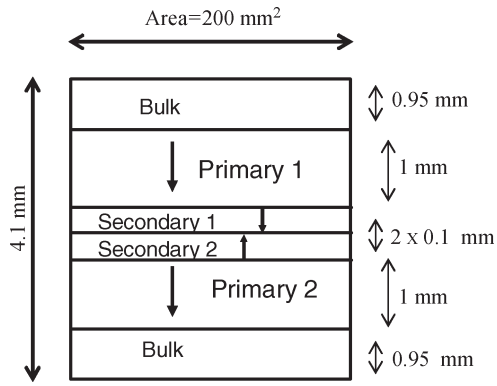

Fig. 7. PT dimensions.

Step 2) Selection of the PT thickness

The operating frequency range of the converter is fixed by the PT in the frequency range located

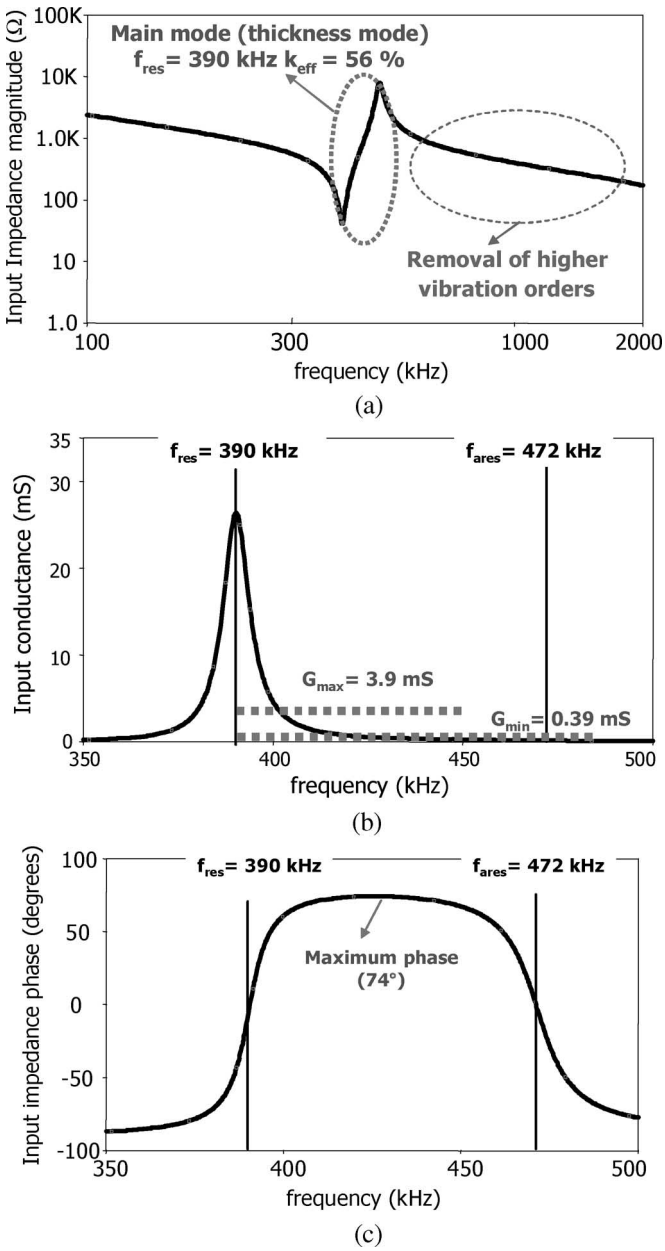

Fig. 8. PT simulated small sample characteristics. (a) Input impedance magnitude with secondary open. (b) Input conductance with its optimum load (12 Ω). (c) Input impedance phase with its optimum load (12 Ω).

between the resonance and antiresonance frequencies, where it is able to transfer energy efficiently and provide a ZVS condition. PT resonance frequency $(f_{\rm res})$ is inversely proportional to the thickness dimension of the device, as is shown in (2), where ρ and c_{33}^D are material properties

$$\text{Thickness} = \frac{1}{2 \cdot f_{\rm res}} \cdot \sqrt{\frac{c_{33}^D}{\rho}}. \qquad (2)$$

Hence, the higher the frequency, the lower the PT size. Nevertheless, the higher the frequency, the higher the switching losses of the converter. Therefore, the optimum switching frequency is a tradeoff between the PT size and the switching losses.

In this particular case, this analysis has not been realized, and the minimum possible frequency due to manufacturing restrictions (maximum thickness is 4 mm) has been selected in order to reduce the switching losses. Taking into account (2), resonance frequency of the PT is around 400 kHz. This frequency is a good tradeoff between size and efficiency.

Step 3) Selection of the electrode area

The maximum PT temperature is determined by a Curie point, where a piezoelectric material loses its properties. Maximum losses require a minimum PT volume to limit the PT temperature rise (ΔT).

Since PT thickness is fixed by the switching frequency, the minimum electrode area is determined by the maximum ΔT.

The peripheral area of the PT (A) has been established in terms of its efficiency $(\eta_{\rm PT})$ and output power $(P_{\rm out,PT})$ by (3), where h [15 W/(m^2 · °C)] is the convection coefficient

$$\Delta T = \frac{1}{h \cdot A}\left(\frac{1}{\eta_{\rm PT}} - 1\right) \cdot P_{\rm out,PT}. \qquad (3)$$

Regarding a previous experience [11], a PT efficiency of 98% and a temperature rise of 55° are determined. By taking into account (3), the minimum electrode area is 60 mm^2.

Step 4) Selection of the electrode distribution

The different electrode distributions have been analyzed in [12]. Interleaving of electrodes that involves placing the secondary electrodes between primary electrodes has been selected since it allows a higher separation of primary electrodes required for the high input voltage of the application. In addition, it removes odd harmonics and allows avoidance of the insulation layer, thereby increasing $\eta_{\rm PT}$ and $k_{\rm eff}$ values.

Step 5) Selection of the thickness and number of secondary layers

The selection of thickness and number of secondary layers is done to adapt the PT design to output conditions. The influence of the load in the behavior of the PT is enormous. The load that implies the maximum PT efficiency is defined as the optimum load $(R_{\rm opt})$. The optimum load of the PT should correspond to the $R_{\rm eq}$ seen by the PT when it is transferring the maximum power. For the selected application, the output load is 14 Ω, and the equivalent value is 12 Ω with a full-wave rectifier $(R_{\rm eq} = (8/\pi^2) \cdot R_{\rm L})$ [6].

The minimum number of secondary layers has been selected in order to reduce the cost. This number is determined by the minimum thickness of the secondary layer, which is limited by the manufacturer to 0.1 mm.

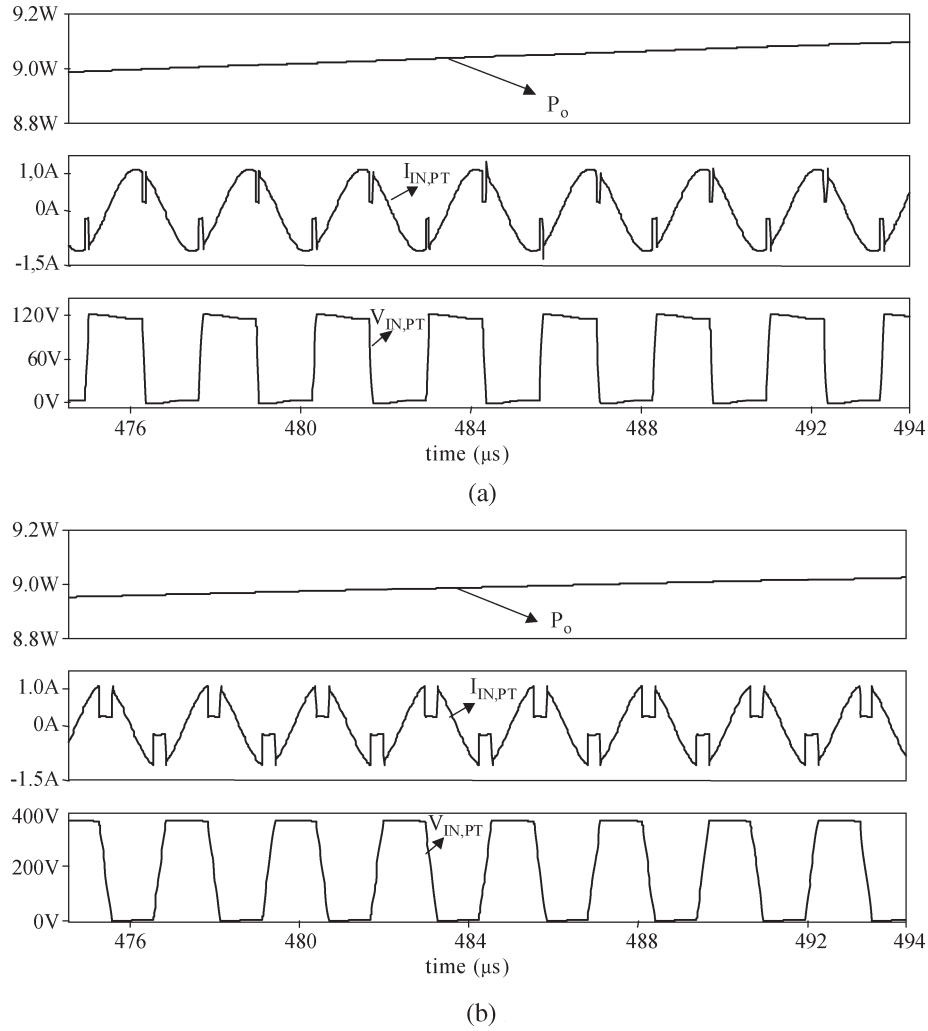

Fig. 9. Analysis of zero voltage switching condition. (a) Minimum input voltage (85 Vrms). (b) Maximum input voltage (265 Vrms).

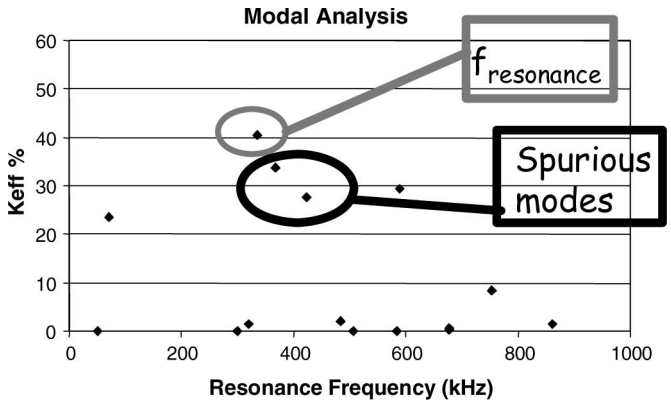

Fig. 10. $k_{\rm eff}$ versus resonance frequency. Bad PT design.

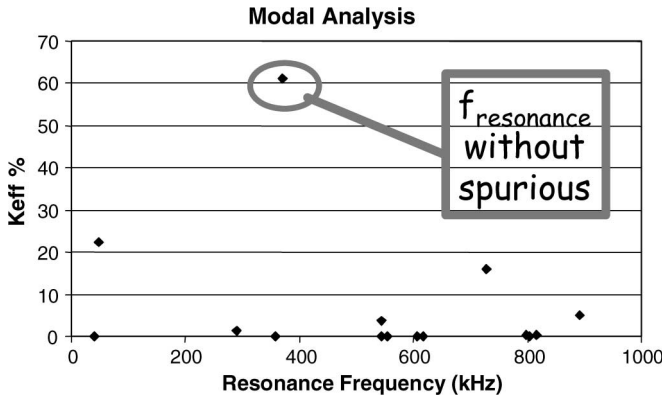

Fig. 11. $k_{\rm eff}$ versus resonance frequency. Good PT design.

Step 6) Selection of the thickness and number of primary layers. Addition of bulks

The selection of thickness and number of primary layers is done to adapt the PT design to input conditions. No poled layers, named as bulk layers, have been added to keep constant the PT thickness.

Since the power that should be transferred by the PT for a given input voltage is a specification, it is necessary to determine what should be the input conductance (real part of the input admittance) of the PT in order to handle the required power (4)

$$P_{\rm in,PT} = V_{\rm in,PT}^2 \cdot G_{\rm in,PT} = \frac{P_{\rm out,PT}}{\eta_{\rm PT}}. \quad (4)$$

In the example, the required $G_{\rm in,PT}$ varies from 0.39 to 3.9 mS to obtain the input voltage variation

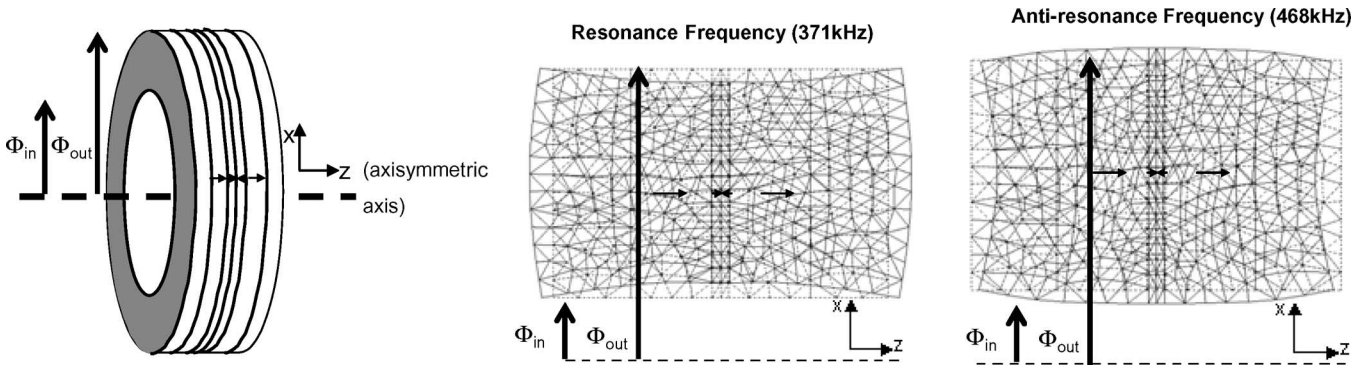

Fig. 12. Axial view of the PT2b vibration in thickness mode. Discontinuous line represents the initial structure, without deformation, and continuous line represents the deformed structure by applying a voltage to the primary side.

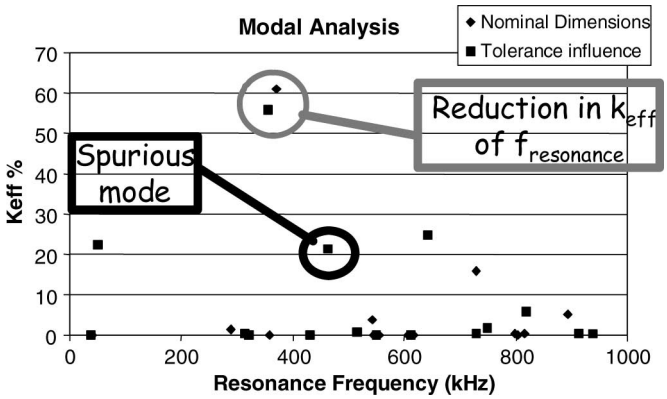

Fig. 13. k_{eff} versus resonance frequency. Tolerances influence on PT.

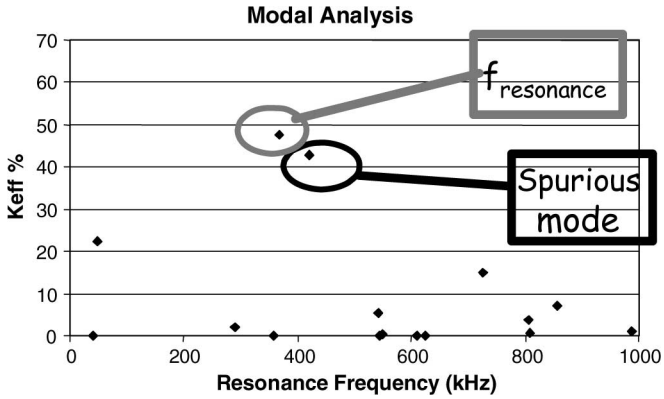

Fig. 15. k_{eff} versus resonance frequency. Free central fixing layer.

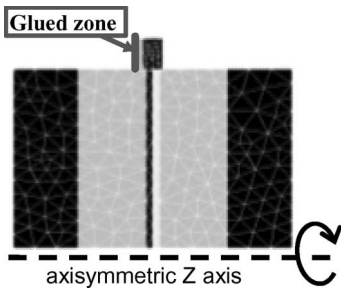

Fig. 14. PT fixed with a belt.

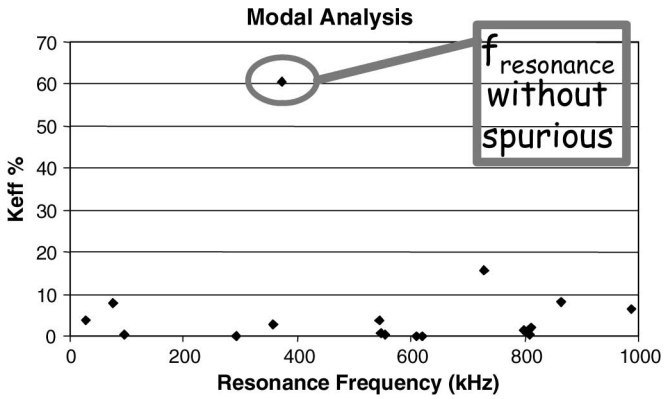

Fig. 16. k_{eff} versus resonance frequency. Glued central fixing layer.

and the power level by considering 50% of the duty cycle and PT and rectifier efficiency of 88%. This efficiency value is reasonable from the point of view of power converter efficiency [11].

Another parameter that must be considered to select the number and thickness of primary layers is the inductive behavior. To design PT with an inductive behavior, when the phase of the input impedance is positive, it allows PT to provide ZVS (Fig. 6).

It is important to highlight that the maximum number of primary layers is limited by PT losses due to the high input voltages. In this particular case, only one primary layer is possible, and there is no thickness of the primary layer that allows achieving a good tradeoff between the required input conductance and the inductive behavior (Table I). Therefore, a reduction in the number of secondary layers is necessary. Unfortunately, as constructive parameters affect several electrical parameters, there is a need to go back to step 3), increasing the area to be able to fulfil all the electrical requirements. From this iterative procedure, an optimized PT design in the thickness direction was obtained. All the PT features have been summarized in Table II and Fig. 7. It has only two layers in the secondary side, but it has an area of 200 mm^2. It allows achieving all the electrical requirements.

1) k_{eff} is high (56%), and there are no higher orders, as the input impedance graph shows [Fig. 8(a)].
2) Optimum load is 12 Ω, as the equivalent load connected to the PT output.

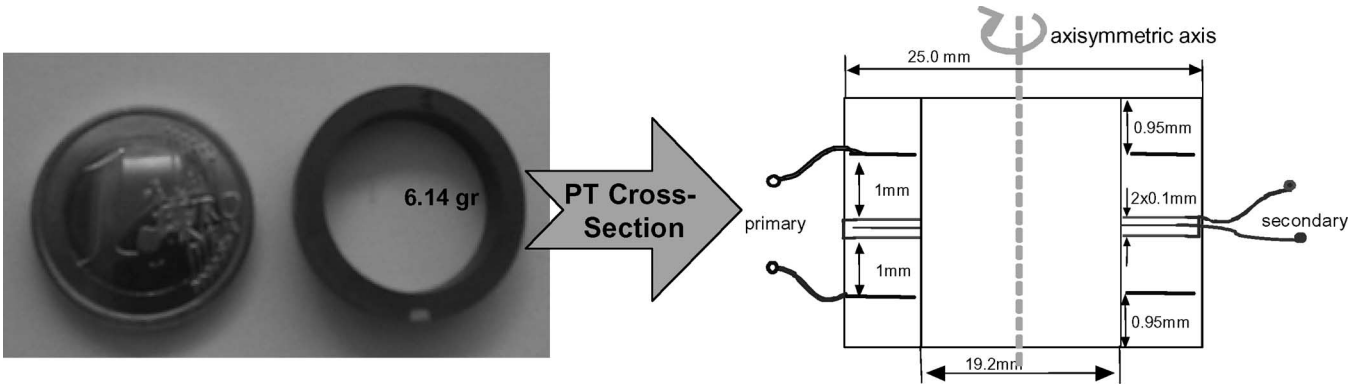

Fig. 17. PT features.

3) Conductance variation [Fig. 8(b)] is achieved inside the operating frequency range.
4) PT has an inductive behavior with a maximum impedance phase of 74° [Fig. 8(c)], and it will present ZVS in the whole voltage range, as simulations show [Fig. 9(a) and (b)].

C. Stage C. 2-D/3-D Design. Geometry Selection

With 1-D analysis, the thickness of each layer and the total area are known, but there are many 3-D possibilities. FEA tools are useful in implementing the 1-D design in a proper 3-D structure design by selecting the geometry with a correct area distribution. There are a lot of geometric possibilities for the PT dimensioning, such as a disc, ring, plate, etc. From the FEA results, it has been deduced, for this kind of PTs made of PZT material and working in thickness mode, that the best geometry is a ring because of the spurious mode reduction at the working frequency range. The FEA tool selected is ATILA [13] because it is specially developed for the simulation of the electromechanical coupling in 2-D/3-D of piezoelectric materials and provides accurate results. This tool has been developed by ISEN, Lille, France.

The selection of the inner $(\phi_{\rm in})$ and outer $(\phi_{\rm out})$ diameters of the ring is also critical. With a bad selection of diameters ($\phi_{\rm out} = 19.73$ mm and $\phi_{\rm in} = 11.61$ mm), there are many spurious modes that are close to the resonance frequency (Fig. 10). On the contrary, by keeping the area constant, if the selection of diameters is right ($\phi_{\rm out} = 24.97$ mm and $\phi_{\rm in} = 19.21$ mm), the working frequency range (between resonance and antiresonance) is clean of spurious modes, and $k_{\rm eff}$ is higher (61%) (Fig. 11). It is necessary to emphasize that finding the correct diameter is not an easy task: For the same area, more than five combinations of $\phi_{\rm out}$ and $\phi_{\rm in}$ have been analyzed, and only one fulfils the requirements. $k_{\rm eff}$ depends not only on the material properties but also on the specific geometry. That is the reason of the difference in FEA $k_{\rm eff}$ (61%), comparing with 1-D model (56%).

Other useful information from FEA is electric field and stress distribution, which limits the PT power density [14]. It is also possible to extract graphics of the displacement for each frequency, which is suitable in understanding the PT's mechanical behavior. In Fig. 12, it is shown that PT vibration between resonance and antiresonance frequencies consists of a compression and expansion along PT thickness (Z-axis), which is the first order of thickness mode, selected for this particular case in order to reduce the switching frequency. This analysis has been done using Cartesian coordinates, and although in the figure it is represented only by the XZ plane, it also takes into account the axial symmetry (being the Z-axisymmetric axis). Cartesian coordinates with axial symmetries are recommended by ATILA software to describe PT structure in order to reduce simulation time.

D. Stage D. Manufacturing Tolerances, Influence on the PT Performance

Manufacturing tolerances must be taken into account in the design process because they may induce new spurious modes and change the $k_{\rm eff}$. It is necessary to achieve a PT design with a working frequency range that is not sensitive to dimension changes caused by the manufacturing tolerances. The piezoelectric material tolerances are about $\pm 3\%$ for the most critical dimension, which is the thickness of each layer. For example, considering a tolerance of -3% in thickness and $\phi_{\rm in}$ and $+3\%$ in $\phi_{\rm out}$, there is a reduction in $k_{\rm eff}$, comparing with the nominal case, and also, a spurious mode appears close to the resonance (Fig. 13). An optimum design must not be too sensitive to these tolerances. In addition, it would be necessary to warn the PT manufacturer about the critical dimensions.

E. Stage E. Fixing Influence on the PT Performance

As it was mentioned before, fixing the PT to the PCB is a critical point because the vibration of the PT can be perturbed, modifying its electrical performance. Fixing can also be used to provide a path for thermal dissipation. Anyway, it is necessary that the fixing method ensures the mechanical robustness of the converter.

For this particular application, it is proposed to add a fixing layer, as a belt, to the PT (Fig. 14). This fixing method makes easier the connection to the PCB with thermal glue and the soldering of wires (if the electrodes are placed in the fixing belt). It also has the advantage of providing a thermal path. The main drawback is that it is very sensitive to the spurious

modes. Therefore, FEA modal analyses are mandatory in the fixing belt design. If the fixing layer is left free, a spurious mode appears near the antiresonance frequency, inducing a wrong movement, and the k_{eff} is also reduced (Fig. 15). However, these problems will disappear if the fixing belt is glued because PT vibrates in the thickness mode and the resonance frequency has no spurious modes in its vicinity (Fig. 16), as it was desired.

III. Experimental Validation

The optimal design is the one that provides the smallest volume (smaller area) with the lowest cost (lower number of electrodes). The design described in Fig. 17 is an optimal PT design that is obtained by following the different design stages described in Section II. As each constructive parameter of the PT has influence in several electrical properties, several iterations in the design process can be required to optimize the PT in order to fulfil all the specifications. It is important to highlight that little changes in the geometrical dimensions are not important from the point of view of electrical parameters. However, these geometrical changes are critical from the point of view of spurious modes. If any dimension changes a bit, spurious modes can appear, as it has been analyzed in Stage D of Section II. PT shape is a ring whose external diameter is of 25 mm and whose internal diameter is of 19 mm to obtain the specified transversal area of 200 mm^2. Total thickness is around 4 mm. It has two electrodes on the secondary side, and the primary contains one at each side (with interleaving of electrodes). This PT was manufactured by Noliac [10].

The first batch of samples has been done without the fixing layer because the manufacturer recommends testing before the PT without it. In this paper, the validation of the design method has been done. Next batch will be manufactured with the fixing layer in order to validate its influence.

Validations with measurements at component and converter levels are presented in this section. Electrical features of the sample obtained by measurements with an impedance analyzer are shown in Fig. 18. They are compared with the simulation results of the proposed design shown in Fig. 8. The main mode (first order of thickness mode) has a k_{eff} of 50% [Fig. 18(a)]. The lower k_{eff} measured value (50%) compared to simulations with 1-D model (56%) [Fig. 8(a)] or FEA (61%) is due to the shape, manufacturing tolerances, and fixing influence, as it has been explained before. It is important to notice that the simulated PT does not consider electrode dimensions, electrode material, and external connection of the electrodes. Hence, a reduction of k_{eff} value in the PT sample is obtained compared to the predicted value, but it is still high enough for the application.

Furthermore, higher vibration orders have been removed owing to the proper electrode distribution, as predicted by the simulations.

The input conductance value [Fig. 18(b)] is achieved (0.39–3.9 mS) inside the operating frequency range that is located between the resonance (f_{res}) and antiresonance (f_{ares}) frequencies. In addition, the expected inductive behavior [maximum phase around 74°, Fig. 8(c)] is obtained [Fig. 18(c)]. Therefore, soft switching transitions (ZVS) without additional

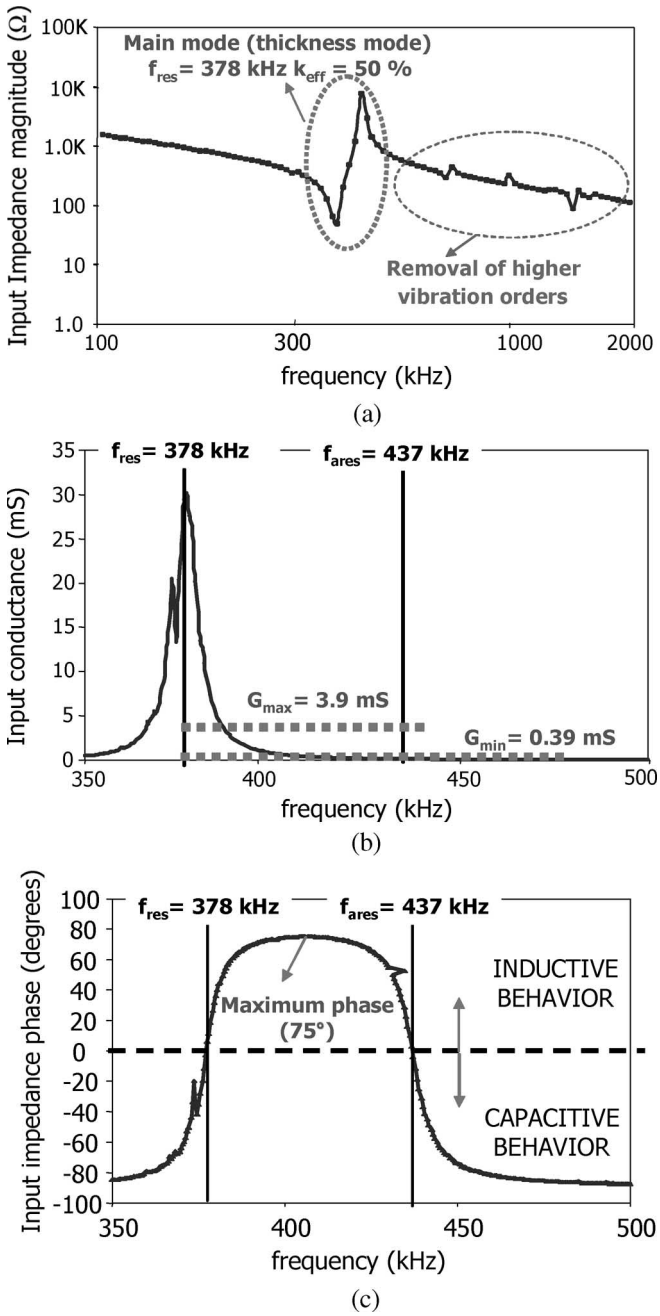

Fig. 18. Measured sample characteristics. (a) Input impedance magnitude with secondary open. (b) Input conductance with its optimum load (12 Ω). (c) Input impedance phase with its optimum load (12 Ω).

magnetic components are obtained, as shown in Fig. 19. However, the penalty of PT design for ZVS is the reduction of its efficiency (93%) and the increment of its size due to the bigger PT area (200 mm^2).

IV. Conclusion

In this paper, a design method for PTs has been proposed and validated at the component and converter levels. It consists of a combination of analytical models and numerical FEA results. It takes into account not only the 1-D effects (with analytical models) but also the 2-D/3-D effects (with FEA tools). Shape, tolerances, and fixing of the PT are the main 2-D/3-D effects

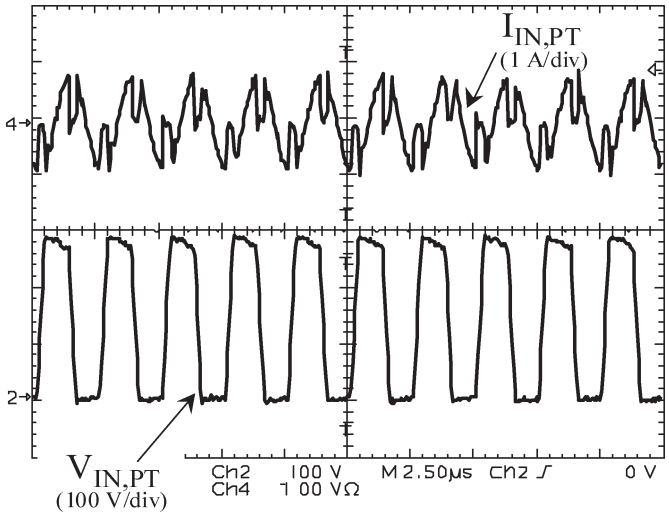

Fig. 19. Input voltage $(V_{\mathrm{in,PT}})$ and current $(I_{\mathrm{in,PT}})$ of the PT in the power converter. $V_{\mathrm{IN}} = 200$ Vef. $P_{\mathrm{o}} = 10$ W.

that must not be forgotten in the design process since they strongly affect its electrical behavior. The proposed design method consists of the following stages:

1) topology selection;
2) analytical modeling and design;
3) 2-D/3-D design and geometry selection;
4) manufacturing tolerances influence on PT performance;
5) fixing layer influence on PT performance.

Since PT design is a complex task, the proposed method makes possible an optimization before manufacturing it, reducing the time and cost of the process. The most important advantage of this PT design method is that it is valid not only for sinusoidal driving but also for square driving. Although square driving penalizes PT performance in terms of size and efficiency, improvements in the whole converter are expected (size) since no magnetic components are needed.

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